CLAIMS

What is claimed is:

1. A method for manufacturing an on-chip inductor comprises:

creating a dielectric layer; and

creating a conductive winding on the dielectric layer, wherein the conductive winding has a substantially square geometry, wherein corners of the conductive winding are geometrically shaped to reduce impedance of the on-chip inductor at an operating frequency.

2. The method of claim 1, wherein the creating of the conductive winding further comprises:

creating the geometric shaping of the corners to include an interior angle per corner of approximately ninety degrees, and an exterior angle per corner of approximately one hundred thirty-five degrees.

3. The method of claim 1, wherein the creating of the conductive winding further comprises:

creating the geometric shaping of the corners to include an interior angle per corner of approximately one hundred thirty-five degrees, and an exterior angle per corner of approximately one hundred thirty-five degrees.

4. The method of claim 1 further comprises:

creating the conductive winding to have a spiral configuration, wherein the corners of the spiral configuration are geometrically shaped to reduce impedance of the on-chip inductor at the operating frequency.

5. The method of claim 1, wherein the creating of the conductive winding further comprises:

creating a first winding on a first layer;

creating a second winding on a second layer; and

connecting the first winding to the second winding with at least one bridge.

6. The method of claim 1, wherein the creating of the conductive winding further comprises:

creating the geometric shaping of the corners to include angled exterior corners, wherein at least one angle per exterior corner reduces current turbulence in the corner at the operating frequency.

7. The on-chip inductor of claim 6, wherein the creating of the conductive winding further comprises:

creating the geometric shaping of the corners to include angled interior corners, wherein at least one angle per interior corner further reduces current turbulence in the corner at the operating frequency.

8. A method of manufacturing an on-chip transformer comprises:

creating primary conductive winding that has a substantially square geometry, wherein corners of the primary conductive winding are geometrically shaped to reduce impedance of the primary conductive winding at an operating frequency; and

creating secondary conductive winding that has a substantially square geometry, wherein corners of the secondary conductive winding are geometrically shaped to reduce impedance of the secondary conductive winding at an operating frequency, wherein the secondary conductive winding is magnetically coupled to the primary conductive winding.

9. The method of claim 8, wherein the creating of the primary and secondary conductive windings further comprises:

creating the geometric shaping of the corners to include an interior angle per corner of approximately ninety degrees, and an exterior angle per corner of approximately one hundred thirty-five degrees.

10. The method of claim 8, wherein the creating of the primary and secondary conductive windings further comprises:

creating the geometric shaping of the corners to include an interior angle per corner of approximately one hundred

thirty-five degrees, and an exterior angle per corner of approximately one hundred thirty-five degrees.

11. The method of claim 8 further comprises:

creating dielectric layer;

creating the primary conductive winding on the dielectric layer, wherein the primary conductive winding includes a spiral configuration, wherein the corners of the spiral configuration are geometrically shaped to reduce impedance of the primary conductive winding at the operating frequency; and

creating the secondary conductive winding on the dielectric layer, wherein the secondary conductive winding includes a secondary spiral configuration interwoven with the spiral configuration of the primary conductive winding, wherein the corners of the secondary spiral configuration are geometrically shaped to reduce impedance of the secondary conductive winding at the operating frequency.

12. The method of claim 8 further comprises:

creating a first dielectric layer;

creating the primary conductive winding on the first dielectric layer, wherein the primary conductive winding includes a spiral configuration, wherein the corners of the spiral configuration are geometrically shaped to reduce impedance of the primary conductive winding at the operating frequency;

creating a second dielectric layer juxtaposed to the primary conductive winding; and

creating the secondary conductive winding on the secondary dielectric layer, wherein the secondary conductive winding includes the spiral configuration, wherein the corners of the spiral configuration are geometrically shaped to reduce impedance of the secondary conductive winding at the operating frequency.

13. The method of claim 8, wherein creating each of the primary and secondary conductive windings further comprises:

creating a first winding on a first layer;

creating a second winding on a second layer; and

connecting the first winding to the second winding with at least one bridge.

14. The method of claim 8, wherein the creating of the primary and secondary conductive windings further comprises:

creating the geometric shaping of the corners to include angled exterior corners, wherein at least one angle per exterior corner reduces current turbulence in the corner at the operating frequency.

15. The method of claim 14, wherein the creating of the primary and secondary conductive windings further comprises:

creating the geometric shaping of the corners to include angled interior corners, wherein at least one angle per interior corner further reduces current turbulence in the corner at the operating frequency.